

REMARKS/ARGUMENTS

Favorable consideration of this application in light of the following discussion is respectfully requested.

Claims 42-49 are pending in the application. Claims 1-41 were cancelled in the preliminary amendment filed on January 6, 2004.

In the outstanding Office Action, Claims 42-49 were rejected under 35 U.S.C. § 112, first paragraph; and Claims 42-49 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Lin (U.S. Patent No. 5,485,428) in view of Kasai et al. (U.S. Patent No. 6,33,948 B2, hereinafter Kasai).

Briefly recapitulating, Claim 42 is directed to a method for reading out a semiconductor memory device. The method includes a) latching data on a data bus into a page latch; and b) transferring the data latched in the page latch to a cell matrix for programming the data at a first mode, and to a read out circuit for reading out the data without programming the data latched in the data latch into the cell matrix at a second mode. Claim 46 is directed to an alternative embodiment of Applicants' invention. Applicants' claimed methods facilitate determining a cause of an error if there is an error in reprogrammed data. The claimed methods also enable rapid testing of page latches and read out circuits.¹

Regarding the rejections under 35 U.S.C. § 112, first paragraph, Applicants note that Claims 42 and 46 are supported by Figures 1a-1b and 16a-16b. That is, both methods include transferring data according to first and second modes. In the first mode, 1) data to be programmed comes in a data latch, 2) the data stored in the data latch is transferred and programmed to a (memory) cell matrix, and then, 3) the data is read out from the cell matrix to the page latch again. In the second mode, 1) data to be programmed comes in the data

¹ Specification, paragraph [00012].

latch, and then, 2) the data stored in the data latch is read out to outside of the semiconductor memory device without programming the data latched in the data latch into the cell matrix. The first mode is used as a test, as one cannot know if the data latch has a defect or not. However, when one uses the second mode, one can specify whether the data latch has the defect or not.² In view of the above discussion and citations to Applicants' originally filed specification, Applicants request the rejections under 35 U.S.C. § 112, first paragraph, be withdrawn. Should further questions exist, the Examiner is respectfully invited to contact Applicants' representative for a personal interview including more detailed review of Applicants' originally filed specification.

Lin discloses a serial access memory device that includes a page select device.³ Kasai discloses a non-volatile memory device that generates check bits as an error correction code.⁴ However, both the 428 and the 948 are silent for the one of the key ideas. Neither the Lin nor Kasai discloses or suggests transferring latched data to a cell matrix according to one mode and transferring data to a read out circuit according to a second mode, as recited in Applicants' original Claims 42 or 46.

As none of the cited prior art, individually or in combination, disclose or suggest all the elements of independent Claims 42 and 46, Applicants submit the inventions defined by Claims 42 and 46, and all claims depending therefrom, are not rendered obvious by the asserted prior art for at least the reasons stated above.⁵

² Specification, paragraph [00064], see also paragraphs [00122-00124].

³ Lin, abstract, Figure 4, col. 5, lines 49-67.

⁴ Kasai, abstract.

⁵ MPEP § 2142 "...the prior art reference (or references when combined) must teach or suggest **all** the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)."

Accordingly, in light of the previous discussion, Applicants respectfully submit that the present application is in condition for allowance and respectfully request an early and favorable action to that effect.

Respectfully submitted,

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